ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

ECET

(Autonomous Institution - UGC, Govt. of India)
(Sponsored by Ellenki Educational Society)
(Approved by AICTE, New Delhi, Affiliated to JNTUH Hyderabad, MSME - HI Govt. of India,
Accredited by NAAC, Recognisation of 2(f) by UGC, ISO 9001:2015 Certified)

UGC AUTONOMOUS

Date: 01-11-2023

Board of Studies of Electronics & Communication Engineering Dept.

On behalf of ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY (Autonomous), Patelguda, Sangareddy-502319. I am pleased to constitute the Board of Studies in the Department of ECE for B.Tech and M.Tech Courses as per details given below:

S.NO	NAME	DESIGNATION	DESIGNATION IN BOS
1	Dr. K.Srinivasulu	Professor & Head Dept.of ECE,ECET	Chairman
2	Dr.A.Rajani	Professor of ECE	JNTUH UCESTH
3	Dr. DMK Chaitanya	Professor ECE, Vasavi College of Engineering	Member
4	Dr. MLN Acharyulu	Professor ECE, CBIT	Member
5	Mr. Bhukya Shankar Rao	Working as Scientist-E in (Defence electronics Research Laboratory) DLRL-DRDO Hyd.	Member
6	Mr. T.Sravan Kumar	Assoc.Professor, ECET	Member
7	Mr.D.Shekar Goud	Assoc.Professor, ECET	Member
8	Mrs.N.Mounika	Assoc.Professor, ECET	Member
9	Mr.M.Srikanth	M.Tech, Alumni	Member
10	Prof. P. John Paul	Principal, ECET	Special Invitee

- The above staff members of the Board of Studies in ECE shall hold the office for a period of three years with effect from the date of issue of this order.
- The members attending the meeting of the Board of Studies are eligible for T.A. and D.A as per rules of the Institution in force.
- The members are also requested to intimate this office in case of any changes in their address and designations.
- We request you to kindly consent your willingness to the member of this BOS.

PRINCIPAL
Ellenki College of Engg. & Tech.
Patelguda (V), Ameenpur (M)
Dist. Sangareddy, 502 319. T.S

Board of studies of Electronics and Communication Engineering Department

Attendance Sheet

In anticipation of approval of the Academic Council, ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY (Autonomous), Patelguda, Sangareddy-502319.I am pleased to constitute the Board of Studies in the Department of ECE for B.Tech and M.Tech Courses as per details given below

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2	Dr.A.Rajani	Professor of ECE	Member -JNTUH	
3	Dr.DMK Chiatanya	Professor of ECE Vasavi College of Engineering	Member- Other college	
4	Dr.MLN Acharyulu	Professor of ECE, CBIT	Member- Other college	
5	Mr.Bhukya Shankar Rao	Working as Scientist-E in (Defence Electronics Reasearch Laboratory)DLRL-DRDO Hyd.	Member-Industry	
6	Mr.T.Sravan Kumar	Assoc.Professor, ECET	Member-College	
7	Mr.D.Shekar Goud	Assoc.Professor, ECET	Member-College	
8	Mrs.N.Mounika	Assoc.Professor, ECET	Member-College	
9	Mr.M.Srikanth	M.Tech, Alumni	Member-Alumini	
10	Prof.P.John Paul	Principal	Special Invitee	

Department of Electronics and communication Engineering

Minutes of Board of Studies Meeting

Date: 15/11/2023

Ellenki College of Engineering & Technology was founded in the year 1999 with a vision to achieve excellence in providing all round education. Established for over two decades, ELLENKI College of Engineering & Technology is one of the premier private engineering colleges in Hyderabad. The College has got Autonomous Status from the A.Y. 2023-24 for a period of 5 years.

The first BOS meeting of Electronics and communication Engineering Department was held on

15th November, 2023 in dual mode. The minutes of meeting are as follows.

The Chairman welcomed all the members for the 1st Board of Studies meeting of the Electronics and communication Engineering Department.

1. Academic course structure for B.Tech (I, II, III & IV year) has been discussed and drafted for ER23 Regulations.
2. Detailed syllabi for B. Tech (I Year) program have been discussed at length. The proposed syllabus has been agreed and no changes were suggested by the BOS members.
3. The proposed syllabus for Electronic Devices & Circuits offering to CSE, CS&DS, CSE(AI&ML) Engineering in I B. Tech II Semester has been approved.
4. Academic course structure for M. Tech (EMBEDDED SYSTEMS), I & II year has been discussed and drafted for ER23 Regulations.
5. Detailed syllabi for M. Tech (EMBEDDED SYSTEMS), I Year program have been discussed at length. The proposed syllabus has been agreed by the BOS Members.

Finally the Chairman thanked to all the members for their presence and also for their valuable suggestions towards the important of the Curriculum and Syllabus of the Electronics and communication Engineering.

Chairman
Board of Studies

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

(AUTONOMUS)

B.Tech. in ELECTRONICS AND COMMUNICATION ENGINEERING
COURSE STRUCTURE, I & II YEAR SYLLABUS (ER23 Regulations)
Applicable from AY 2023-24 Batch

I Year I Semester

S. No.	Course Code	Course Title	L	T	P	Credits
1.	ER23MA1101	Matrices and Calculus	3	1	0	4
2.	PH1102	Applied Physics	3	1	0	4
3.	CS1104	C Programming for Engineers	3	0	0	3
4.	ME1104	Engineering Workshop	0	1	3	2.5
5.	EN1105	English for Skill Enhancement	2	0	0	2
6.	EC1106	Elements of Electronics and Communication Engineering	0	0	2	1
7.	PH1107	Applied Physics Laboratory	0	0	3	1.5
8.	CS1108	C Programming for Engineers Laboratory	0	0	2	1
9.	EN1108	English Language and Communication Skills Laboratory	0	0	2	1
10.	*MC1101	Environmental Science	3	0	0	0
		Induction Programme				
		Total	**14**	**3**	**12**	**20**

I Year II Semester

S. No.	Course Code	Course Title	L	T	P	Credits
1.	ER23MA1201	Ordinary Differential Equations and Vector Calculus	3	1	0	4
2.	CH1202	Engineering Chemistry	3	1	0	4
3.	ME1203	Computer Aided Engineering Graphics	1	0	4	3
4.	EE1204	Basic Electrical Engineering	2	0	0	2
5.	EC1205	Electronic Devices and Circuits	2	0	0	2
6.	CS1207	Applied Python Programming Laboratory	0	1	2	2
7.	CH1207	Engineering Chemistry Laboratory	0	0	2	1
8.	EE1208	Basic Electrical Engineering Laboratory	0	0	2	1
9.	EC1209	Electronic Devices and Circuits Laboratory	0	0	2	1
		Total	**11**	**3**	**12**	**20**

II YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1		Numerical Methods and Complex Variables	3	1	0	4
2		Analog Circuits	3	0	0	3
3		Network analysis and Synthesis	3	0	0	3
4		Digital Logic Design	3	0	0	3
5		Signals and Systems	3	1	0	4
6		Analog Circuits Laboratory	0	0	2	1
7		Digital logic Design Laboratory	0	0	2	1
8		Basic Simulation Laboratory	0	0	2	1
9	*MC	Constitution of India	3	0	0	0
		Total Credits	**18**	**2**	**6**	**20**

II YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1		Probability Theory and Stochastic Processes	3	0	0	3
2		Electromagnetic Fields and Transmission Lines	3	0	0	3
3		Analog and Digital Communications	3	0	0	3
4		Linear and Digital IC Applications	3	0	0	3
5		Electronic Circuit Analysis	3	0	0	3
6		Analog and Digital Communications Laboratory	0	0	2	1
7		Linear and Digital IC Applications Laboratory	0	0	2	1
8		Electronic Circuit Analysis Laboratory	0	0	2	1
9		Real Time Project/ Field Based Project	0	0	4	2
10	*MC	Gender Sensitization Lab	0	0	2	0
		Total Credits	**15**	**0**	**12**	**20**

III YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1		Microcontrollers	3	1	0	4
2		IoT Architectures and Protocols	3	0	0	3
3		Control Systems	3	1	0	4
4		Business Economics & Financial Analysis	3	0	0	3
5		Professional Elective – I	3	0	0	3
6		Microcontrollers Laboratory	0	0	2	1
7		IoT Architectures and Protocols Laboratory	0	0	2	1
8		Advanced English Communication Skills Laboratory	0	0	2	1
9	*MC	Intellectual Property Rights	3	0	0	0
		Total Credits	**18**	**2**	**6**	**20**

III YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1		Antennas and Wave Propagation	3	0	0	3
2		Digital Signal Processing	3	0	0	3
3		CMOS VLSI Design	3	0	0	3
4		Professional Elective - II	3	0	0	3
5		Open Elective – I	3	0	0	3
6		Digital Signal Processing Laboratory	0	0	2	1
7		CMOS VLSI Design Laboratory	0	0	2	1
8		Advanced Communication Laboratory	0	0	2	1
9		Industry Oriented Mini Project/ Internship	0	0	4	2
10	*MC	Environmental Science	3	0	0	0
		Total Credits	**18**	**0**	**10**	**20**

Environmental Science in III Yr II Sem Should be Registered by Lateral Entry Students Only.

IV YEAR I SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1		Microwave and Optical Communications	3	1	0	4
2		Professional Elective – III	3	0	0	3
3		Professional Elective – IV	3	0	0	3
4		Open Elective – II	3	0	0	3
5		Professional Practice, Law & Ethics	3	0	0	2
6		Microwave and Optical Communications Laboratory	0	0	4	2
7		Project Stage – I	0	0	6	3
		Total Credits	**15**	**1**	**10**	**20**

IV YEAR II SEMESTER

S. No.	Course Code	Course Title	L	T	P	Credits
1		Professional Elective – V	3	0	0	3
2		Professional Elective – VI	3	0	0	3
3		Open Elective – III	3	0	0	3
4		Project Stage – II including Seminar	0	0	22	11
		Total Credits	**9**	**0**	**22**	**20**

***MC – Satisfactory/Unsatisfactory**

Professional Elective – I

EC511PE	Computer Organization & Operating Systems
EC512PE	Data Communications and Computer Networks
EC513PE	Electronic Measurements and Instrumentation

Professional Elective – II

EC611PE	Digital Image Processing
EC612PE	Mobile Communications and Networks
EC613PE	Embedded System Design

Professional Elective – III

EC711PE	Radar Systems
EC712PE	CMOS Analog IC Design
EC713PE	Artificial Neural Networks

Professional Elective – IV

EC721PE	Network Security and Cryptography
EC722PE	Satellite Communications
EC723PE	Biomedical Instrumentation

Professional Elective – V

EC811PE	Artificial Intelligence
EC812PE	5G and beyond Communications
EC813PE	Machine learning

Professional Elective – VI

EC821PE	Multimedia Database Management Systems

EC822PE	System on Chip Architecture
EC823PE	Wireless sensor Networks

Open Electives

Open Elective (OE – I)	Open Elective (OE - II)	Open Elective (OE – III)
1. Fundamentals of Internet of Things 2. Principles of Signal Processing 3. Digital Electronics for Engineering	1. Electronic Sensors 2. Electronics for Health Care 3. Telecommunications for Society	1. Measuring Instruments 2. Communication Technologies 3. Fundamentals of Social Networks

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

(AUTONOMUS)

M.TECH IN EMBEDDED SYSTEMS

PROPOSED COURSESTRUCTURE (ER23Regulations)
EFFECTIVE FROM ACADEMIC YEAR 2023-24 ADMITTED BATCH

ER23 COURSE STRUCTURE AND SYLLABUS

I YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
ER23ES6101	Digital System Design with FPGAs	3	0	0	3
ER23ES6102	System Design with Embedded Linux	3	0	0	3
ER23ES6103 ER23ES6104 ER23ES6105	1. CMOS VLSI Design 2. Pattern Recognition and Machine Learning 3. Wireless Sensor Networks	3	0	0	3
ER23ES6106 ER23ES6107 ER23ES6108	1. Communications Buses & Interfaces 2. Advanced Computer Architecture 3. CMOS Analog IC Design	3	0	0	3
ER23ES6109	Digital system Design with FPGAs Lab	0	0	4	2
ER23ES6110	System Design with Embedded Linux Lab	0	0	4	2
	Research Methodology & IPR	2	0	0	2
AC6101	Audit Course – I	2	0	0	0
	Total	**16**	**0**	8	**18**

I YEAR II – SEMESTER

Course Code	Course Title	L	T	P	Credits
ER23ES6201	ARM Microcontrollers	3	0	0	3
ER23ES6202	Digital Control Systems	3	0	0	3
ER23ES6203 ER23ES6204 ER23ES6205	1. IoT Architectures and System Design 2. Design for Testability 3. SoC Design	3	0	0	3
ER23ES6206 ER23ES6207 ER23ES6208	1. Hardware and Software Co-Design 2. Secure Networks 3. Physical Design Automation	3	0	0	3
ER23ES6209	ARM Microcontrollers Lab	0	0	4	2
ER23ES6210	Digital Control Systems Lab	0	0	4	2
ER23ES6211	Seminar	0	0	4	2
AC6201	Audit Course – II	2	0	0	0
	Total	**14**	**0**	**12**	**18**

II YEAR I – SEMESTER

Course Code	Course Title	L	T	P	Credits
	1. Embedded Networks 2. CMOS Mixed Signal Design 3. Human -Machine Interface	3	0	0	3
	Open Elective	3	0	0	3
	Dissertation Work Review – II	0	0	12	6
	Total	**6**	**0**	**12**	**12**

II YEAR II - SEMESTER

Course Code	Course Title	L	T	P	Credits
	Dissertation Work Review - III	0	0	12	06
	Dissertation Viva-Voce	0	0	28	14
	Total	**0**	**0**	**40**	**20**

Open Electives:

1. Business Analytics
2. Industrial Safety
3. Operations Research
4. Cost Management of Engineering Projects
5. Composite Materials

Audit Course I & II:

1. English for Research Paper Writing
2. Disaster Management
3. Sanskrit for Technical Knowledge
4. Value Education
5. Constitution of India
6. Pedagogy Studies
7. Stress Management by Yoga
8. Personality Development Through Life Enlightenment Skills

ELEMENTS OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech. I Year I Sem.

L	T	P	C
0	0	2	1

Course outcomes: Students will be able to:

1. Identify the different components used for electronics applications
2. Measure different parameters using various measuring instruments
3. Distinguish various signal used for analog and digital communications

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	1	1	1	-	-	1	-	-	1
CO2	3	2	3	2	1	2	-	-	1	-	-	1
CO3	3	3	2	1	1	2	-	-	1	-	-	1

List of Experiments:

1. Understand the significance of Electronics and communications subjects
2. Identify the different passive and active components
3. Color code of resistors, finding the types and values of capacitors
4. Measure the voltage and current using voltmeter and ammeter
5. Measure the voltage, current with Multimeter and study the other measurements using Multimeter
6. Study the CRO and measure the frequency and phase of given signal
7. Draw the various Lissajous figures using CRO
8. Study the function generator for various signal generations
9. Study of Spectrum analyzer and measure the spectrum
10. Operate Regulated power supply for different supply voltages
11. Study the various gates module and write down the truth table of them
12. Identify various Digital and Analog ICs
13. Observe the various types of modulated signals.
14. Know the available Softwares for Electronics and communication applications

ELECTRONIC DEVICES AND CIRCUITS

B.Tech. I Year II Sem.

L	T	P	C
2	0	0	2

Course Objectives:

1. To introduce components such as diodes, BJTs and FETs.
2. To know the applications of devices.
3. To know the switching characteristics of devices.

Course Outcomes: Upon completion of the Course, the students will be able to:

1. Acquire the knowledge of various electronic devices and their use on real life.
2. Know the applications of various devices.
3. Acquire the knowledge about the role of special purpose devices and their applications.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	1	2	-	-	1	1	-	-	-	-	1
CO2	3	2	3	-	-	2	1	-	-	-	-	1
CO3	3	3	3	-	-	2	1	-	-	-	-	1

UNIT - I

Diodes: Diode - Static and Dynamic resistances, Equivalent circuit, Diffusion and Transition Capacitances, V-I Characteristics, Diode as a switch- switching times.

UNIT - II

Diode Applications: Rectifier - Half Wave Rectifier, Full Wave Rectifier, Bridge Rectifier, Rectifiers with Capacitive and Inductive Filters, Clippers-Clipping at two independent levels, Clamper-Clamping Circuit Theorem, Clamping Operation, Types of Clampers.

UNIT - III

Bipolar Junction Transistor (BJT): Principle of Operation, Common Emitter, Common Base and Common Collector Configurations, Transistor as a switch, switching times,

UNIT - IV

Junction Field Effect Transistor (FET): Construction, Principle of Operation, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, FET as Voltage Variable Resistor, MOSFET, MOSTET as a capacitor.

UNIT – V

Special Purpose Devices: Zener Diode - Characteristics, Zener diode as Voltage Regulator, Principle of Operation - SCR, Tunnel diode, UJT, Varactor Diode, Photo diode, Solar cell, LED, Schottky diode.

TEXT BOOKS:

1. Jacob Millman - Electronic Devices and Circuits, McGraw Hill Education
2. Robert L. Boylestead, Louis Nashelsky- Electronic Devices and Circuits theory, 11th Edition, 2009, Pearson.

REFERENCE BOOKS:

1. Horowitz -Electronic Devices and Circuits, David A. Bell – 5thEdition, Oxford.
2. Chinmoy Saha, Arindam Halder, Debaati Ganguly - Basic Electronics-Principles and Applications, Cambridge, 2018.

ELECTRONIC DEVICES AND CIRCUITS LABORATORY

B.Tech. I Year II Sem.

L	T	P	C
0	0	2	1

Course Outcomes: Students will be able to

1. Acquire the knowledge of various semiconductor devices and their use in real life.
2. Design aspects of biasing and keep them in active region of the device for functional circuits
3. Acquire the knowledge about the role of special purpose devices and their applications.

Course	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	-	2	-	3	-	-	3	3	-	-	1
CO2	1	-	2	-	3	-	-	3	3	-	-	1
CO3	1	-	2	-	3	-	-	3	3	-	-	1

List of Experiments (Twelve experiments to be done):

Verify any twelve experiments in H/W Laboratory

1. PN Junction diode characteristics A) Forward bias B) Reverse bias.
2. Full Wave Rectifier with & without filters
3. Types of Clippersat different reference voltages
4. Types of Clampers at different reference voltages
5. The steady state output waveform of clampers for a square wave input
6. Input and output characteristics of BJT in CB Configuration
7. Input and output characteristics of BJT in CE Configuration
8. Input and output characteristics of BJT in CC Configuration
9. Input and output characteristics of MOS FET in CS Configuration
10. Input and output characteristics of MOS FET in CD Configuration
11. Switching characteristics of a transistor
12. Zener diode characteristics and Zener as voltage Regulator
13. SCR Characteristics.
14. UJT Characteristics and identify negative region
15. Photo diode characteristics
16. Solar cell characteristics
17. LED Characteristics

*Design a circuit to switch on and off LED using diode/BJT/FET as a switch.

Major Equipment required for Laboratories:

1. Regulated Power Suppliers, 0-30V
2. 20 MHz, Dual Channel Cathode Ray Oscilloscopes.
3. Functions Generators-Sine and Square wave signals
4. Multimeters, voltmeters and Ammeters
5. Electronic Components and devices

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
DIGITAL SYSTEM DESIGN WITH FPGAs (PC – I)

Pre-Requisite: Switching Theory and Logic Design

Course Objectives:

1. To provide extended knowledge of digital logic circuits in the form of state model approach.
2. To provide an overview of system design approach using programmable logic devices.
3. To provide and understand of fault models and test methods.
4. To get exposed to the various architectural features of CPLDS and FPGAS.
5. To learn the methods and techniques of CPLD & FPGA design with EDA tools.
6. To expose software tools used for design process with the help of case studies.

Course Outcomes:

1. To exposes the design approaches using FPGAs.
2. To provide in depth understanding of Fault models.
3. To understands test pattern generation techniques for fault detection.
4. To design fault diagnosis in sequential circuits.
5. To provide understanding in the design of flow using case studies.

UNIT - I

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, FPGAs-FPGA technology, architecture, virtex CLB and slice, FPGA Programming Technologies, Xilinx XC2000, XC3000, XC4000 Architectures, Actel ACT1, ACT2 and ACT3 Architectures. [TEXTBOOK-1]

UNIT - II

Analysis and derivation of clocked sequential circuits with state graphs and tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation. Need and Design stratagies for multi-clock sequential circuits. [TEXTBOOK-2]

UNIT - III

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Controller (FSM) – Metastability, Synchronization, FSM Issues, Pipelining resources sharing, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design. [TEXTBOOK-2]

UNIT - IV

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.

Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults. [TEXTBOOK-3 & Ref.1]

UNIT - V

Fault Diagnosis in sequential circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment. [Ref.3]

TEXT BOOKS

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth, Jr. -5th Ed., Cengage Learning.
3. Digital Circuits and Logic Design-Samuel C. LEE, PHI, 2008.

REFERENCE BOOKS

1. Logic Design Theory-N.N. Biswas, PHI.
2. Digital System Design using programmable logic devices- Parag K. Lala, BS publications.
3. Switching and Finite Automata Theory - Zvi Kohavi & Niraj K. Jha, 3rd Edition, Cambridge, 2010.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
SYSTEM DESIGN WITH EMBEDDED LINUX (PC – II)

Course Objectives:

1. To know the difference between Embedded Linux and Desktop Linux
2. To understand the kernel concepts of Embedded Linux
3. To learn the debugging, writing, profile applications and drivers in embedded Linux.

Course Outcomes: At the end of this course, students will be able to

1. Familiarity of the embedded Linux development model.
2. Write, debug, and profile applications and drivers in embedded Linux.
3. Create Linux BSP for a hardware platform

UNIT- I

Introduction to Real Time Operating Systems: Characteristics of RTOS, Tasks Specifications and types, Real-Time Scheduling Algorithms, Concurrency, Inter-process Communication and Synchronization mechanisms, Priority Inversion, Inheritance and Ceiling. Embedded Linux Vs Desktop Linux, Embedded Linux Distributions, System calls, Static and dynamic libraries, Cross tool chains

UNIT- II

Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence

UNIT- III

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Device Drivers: Communication between user space and kernel space drivers, Character and Block Device Drivers, Interrupt handling, Kernel modules
Embedded Drivers: Serial, Ethernet, I2 C, USB, Timer, Kernel Modules

UNIT- IV

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux

UNIT- V

Building and Debugging: Bootloaders, Kernel, Root file system, Device Tree

TEXT BOOKS:

1. Chris Simmonds, "Mastering Embedded Linux Programming" - Second Edition, PACKT Publications Limited.
2. Karim Yaghmour, "Building Embedded Linux Systems", O'Reilly & Associates
3. P Raghvan, Amol Lad, Sriram Neelakandan, "Embedded Linux System Design and Development", Auerbach Publications

REFERENCE BOOKS:

1. Christopher Hallinan, "Embedded Linux Primer: A Practical Real-World Approach", Prentice Hall, 2nd Edition, 2010.
2. Derek Molloy, "Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER

EMBEDDED SYSTEMS

CMOS VLSI DESIGN (PE - I)

Course Objectives:

1. To understand the concepts of MOS Design and transient response
2. To know the design of combinational MOS logic circuits
3. To know the design of sequential MOS logic circuits
4. To understand the dynamic logic and also memory designing

Course Outcomes: Students will be able to:

1. Design of combinational MOS logic and sequential MOS logic circuits
2. Design of different Memories using MOS transistors
3. Design a circuits based on dynamic logic
4. Use CMOS transmission gates in various applications

UNIT - I

MOS Design

Pseudo NMOS logic- Inverter, Inverter threshold voltage, output high voltage, Output lowvoltage, gain at gate threshold voltage, transient response, rise time, fall time, pseudo NMOS logic gates, transistor equivalency, CMOS inverter logic.

UNIT - II

Combinational MOS logic circuits

MOS logic circuits with NMOS loads, Primitive CMOS logic gates- NOR and NAND gates, Complex logic circuits design- realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full-adder, CMOS transmission gates, designing with transmission gates.

UNIT - III

Sequential MOS logic circuits: Behavior of bistable elements, SR Latch, Clocked Latch and Flip-flop circuits, CMOS D Latch and edge triggered flip-flop.

UNIT - IV

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, high performance dynamic CMOS circuits.

UNIT - V

Semiconductor Memories: Types, RAM array Organization, DRAM- types, operation, leakage currents in DRAM cell and refresh operation, SRAM - operation, leakage currents in SRAM cells, Flash memory- NOR flash and NAND flash.

TEXT BOOKS:

1. Digital Integrated Circuit Design- Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuit Analysis and Design – Sung Mo Kang, YusufLeblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective- Ming Bo Lin,CRC Press, 2011.
2. Digital Integrated Circuits: A Designs Perspective -Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
PATTERN RECOGNITION AND MACHINE LEARNING (PE – I)

Prerequisite: Statistics and Linear Algebra

Course Objectives:

1. The student will be able to understand the mathematical formulation of patterns.
2. To study the various linear models.
3. Understand the basic classifiers.
4. Can able to distinguish different models.

Course Outcomes: On completion of this course student will be able to

1. Familiar the basics of pattern classes and functionality.
2. Construct the various linear models.
3. Use the different kernel methods.
4. Design the Markov and Mixed models.

UNIT-I

Introduction to Pattern recognition: Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization

UNIT-II

Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs, Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models -Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

UNIT-III

Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity, RVM for classification

UNIT-IV

Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, D-separation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.

UNIT-V

Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM-Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.

TEXT BOOKS:

1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press, volume no.52.
2. Pattern Recognition and Machine Learning- C. Bishop-Springer,2006.

REFERENCE BOOKS:

1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd Ed., 2001.
2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, Springer, 2nd Ed., 2009.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
WIRELESS SENSOR NETWORKS (PE –I)

Course Objectives

1. To acquire the knowledge about various architectures and applications of Sensor Networks
2. To understand issues, challenges and emerging technologies for wireless sensor networks
3. To learn about various routing protocols and MAC Protocols
4. To understand various data gathering and data dissemination methods
5. To Study about design principals, node architectures, hardware and software required for implementation of wireless sensor networks.

Course Outcomes: Upon completion of the course, the student will be able to:

1. Analyze and compare various architectures of Wireless Sensor Networks
2. Understand Design issues and challenges in wireless sensor networks
3. Analyze and compare various data gathering and data dissemination methods.
4. Design, Simulate and Compare the performance of various routing and MAC protocol

UNIT -I:

Introduction to Sensor Networks, unique constraints and challenges, Advantage of Sensor Networks, Applications of Sensor Networks, Types of wireless sensor networks

UNIT –II

Mobile Ad-hoc Networks (MANETs) and Wireless Sensor Networks, Enabling technologies for Wireless Sensor Networks. Issues and challenges in wireless sensor networks

UNIT –III

Routing protocols, MAC protocols: Classification of MAC Protocols, S-MAC Protocol, B-MAC protocol, IEEE 802.15.4 standard and ZigBee

UNIT -IV

Dissemination protocol for large sensor network. Data dissemination, data gathering, and data fusion; Quality of a sensor network; Real-time traffic support and security protocols.

UNIT -V

Design Principles for WSNs, Gateway Concepts Need for gateway, WSN to Internet Communication, and Internet to WSN Communication. Single-node architecture, Hardware components & design constraints, Operating systems and execution environments, introduction to TinyOS and nesC.

TEXT BOOKS:

1. Ad-Hoc Wireless Sensor Networks- C. Siva Ram Murthy,B. S. Manoj, Pearson
2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

REFERENCE BOOKS:

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Wireless Communications-Andrea Goldsmith, 2005 Cambridge University Press.
3. Mobile Cellular Communication – Gottapu Sasibhushana Rao, Pearson Education, 2012.
4. Wireless Communication and Networking – William Stallings, 2003, PHI.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER

EMBEDDED SYSTEMS

COMMUNICATION BUSES AND INTERFACES (PE - II)

Course Objectives:

1. To know how to select the suitable Buses for different applications
2. To know the architecture of CAN and applications
3. To understand the use of PCIe, USB etc.,
4. To know the serial communication protocol

Course Outcomes: At the end of the course, students will be able to:

1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT - I

Serial Busses - Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I2C, SPI

UNIT - II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT - III

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT - IV

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT - V

Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable

TEXT BOOKS:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition
2. Jan Axelson, "USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 –200x
6. Technical references onwww.can-cia.org, http://www.pcisig.com/www.pcisig.com, http://www.usb.org/www.usb.org

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER

EMBEDDED SYSTEMS

COMMUNICATION BUSES AND INTERFACES (PE - II)

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3. Design and develop peripherals that can be interfaced to desired serial bus.

UNIT - I

Serial Busses - Physical interface, Data and Control signals, features, limitations and applications of RS232, RS485, I2C, SPI

UNIT - II

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT - III

PCIe - Revisions, Configuration space, Hardware protocols, applications

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2. Jan Axelson, "USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 –200x
6. Technical references onwww.can-cia.org, http://www.pcisig.com/www.pcisig.com, http://www.usb.org/www.usb.org

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
ADVANCED COMPUTER ARCHITECTURE (PE – II)

Course Objectives:

1. To understand the fundamental of computer design
2. To know the pipelines and parallelism concepts
3. To know the issues in interconnect networks

Course Outcomes: At the end of the course, students will be able to:

1. Familiarize the instruction set, memory addressing of Computer
2. Handle the issues in pipelining and parallelism
3. Familiarize the practical issues in inter network

UNIT - I

Fundamentals of Computer Design: Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT - II

Pipelines: Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design: Introduction, review of ABC of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT - III

Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach: Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT - IV

Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT - V

Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls

TEXT BOOK:

1. John L. Hennessy, David A. Patterson, "Computer Architecture: A Quantitative Approach", 3rd Edition, Elsevier.

REFERENCE BOOKS:

1. John P. Shen and Miikko H. Lipasti, "Modern Processor Design: Fundamentals of Super Scalar Processors", 2002, Beta Edition, McGraw-Hill
2. Kai Hwang, Faye A.Brigs., "Computer Architecture and Parallel Processing", Mc Graw Hill.
3. DezsoSima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architecture - A Design Space Approach", Pearson Education.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
CMOS ANALOG IC DESIGN (PE -II)

Pre-requisite: Analog Electronics

Course Objectives: Analog circuits play a very crucial role in all electronic systems and due to continuedminiaturization, many of the analog blocks are not getting realized in CMOS technology.

1. To understand most important building blocks of all CMOS analog Ics.
2. To study the basic principle of operation, the circuit choices and the tradeoffs involved in theMOS transistor level design common to all analog CMOS ICs.
3. To understand specific design issues related to single and multistage voltage, current anddifferential amplifiers, their output and impedance issues, bandwidth, feedback and stability.
4. To understand the design of differential amplifiers, current amplifiers and OP AMPs.

Course Outcomes: After studying the course, each student is expected to be able to

1. Design basic building blocks of CMOS analog ICs.
2. Carry out the design of single and two stage operational amplifiers and voltage references.
3. Determine the device dimensions of each MOSFETs involved.
4. Design various amplifiers like differential, current and operational amplifiers.

UNIT - I
MOS Devices and Modeling
The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small- Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT- II
Analog CMOS Sub-Circuits
MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors- Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT – III
CMOS Amplifiers
Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT - IV
CMOS Operational Amplifiers
Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps,Power-Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT - V
Comparators
Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS:

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford UniversityPress, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS:

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013.
2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
DIGITAL SYSTEM DESIGN WITH FPGAs LAB (Lab – I)

Part –I:

Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of Full Adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of Combinational circuit using Decoders.
4. Design of Combinational circuit using encoder (without and with parity).
5. Design of Combinational circuit using multiplexer.
6. Design of 4 bit binary to gray converter using MUX or Decoders.
7. Design of Multiplexer/ Demultiplexer, comparator in all 3 styles.
8. Modelling of an Edge triggered and Level triggered FFs : D, SR, JK
9. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
10. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out using different FFs.
11. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
12. Design of 4- Bit Multiplier, Divider.
13. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment,
14. Implementing the above designs on FPGA kits.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY
M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
SYSTEM DESIGN WITH EMBEDDED LINUX LAB (Lab – II)

List of Experiments:

1. **Functional Testing Of Devices:** Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. **Exporting Display On To Other Systems:** Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. **GPIO Programming:** Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. **Interfacing Chronos eZ430:** Chronos device is a programmable texas instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. **ON/OFF Control Based On Light Intensity:** Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. **Battery Voltage Range Indicator:** Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 led's, turn on 3 led's for 2-3V, 2 led's for 1-2V, 1 led for 0.1-1V & turn off all for 0V)
7. **Dice Game Simulation:** Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. **Displaying RSS News Feed On Display Interface:** Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. **Porting Openwrt To the Device:** Attempt to use the device while connecting to a wifi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. **Hosting a website on Board:** Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.
11. **Webcam Server:** Interfacing the regular usb webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. **FM Transmission:** Transforming the device into a regular fm transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Note: Devices mentioned in the above lists include Arduino, Raspbery Pi, Beaglebone

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- I SEMESTER
EMBEDDED SYSTEMS
RESEARCH METHODOLOGY AND IPR

Course Objectives:

- To understand the research problem
- To know the literature studies, plagiarism and ethics
- To get the knowledge about technical writing
- To analyze the nature of intellectual property rights and new developments
- To know the patent rights

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT- I:
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.
Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT- II:
Effective literature studies approaches, analysis, Plagiarism, Research ethics

UNIT- III:
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT- IV:
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT- V:
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications. New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

TEXT BOOKS:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

REFERENCE BOOKS:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in New Technological Age", 2016.
7. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER

EMBEDDED SYSTEMS

ARM MICROCONTROLLERS (PC -III)

Prerequisite: Microprocessors and Microcontrollers

Course Objectives:

1. Explore the architecture and instruction set of ARM processor.
2. To provide a comprehensive understanding of various programs of ARM Processors.
3. Learn the programming on ARM Cortex M.

Course Outcomes: After completing this course the student will be able to:

1. Explore the selection criteria of ARM processors by understanding the functional level trade off issues.
2. Explore the ARM development towards the functional capabilities.
3. Work with ASM level program using the instruction set.
4. Programming the ARM Cortex M.

UNIT - I

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions, Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT - II

Introduction to the Arm Instruction Set: Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT - III

Technical Details of ARM Cortex M Processors General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors- Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT - IV

Instruction SET of ARM Cortex M Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT -V

Floating Point Operations About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

TEXT BOOKS:

1. Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT- ARM System Developer's Guide Designing and Optimizing System Software, Elsevier Publications, 2004.
2. Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Elsevier Publications, 3rd Ed.,

REFERENCE BOOKS:

1. Steve Furber - Arm System on Chip Architectures –Edison Wesley, 2000.
2. David Seal - ARM Architecture Reference Manual, Edison Wesley, 2000.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
DIGITAL CONTROL SYSTEMS (PC -IV)

Prerequisite: Control Systems

Course Objectives:

1. To understand the fundamentals of digital control systems representations, z-transforms
2. To understand analysis of discrete complex domain: Z-Transforms
3. To understand the concepts of state variables analysis for discrete LTIV systems.
4. To understand the concepts of controllability and observability of discrete time systems
5. To get exposed the design aspects of controllers and for discrete time systems
6. To understand the concepts of the stability for discrete LTIV systems
7. To understand the design aspects of observers for discrete time systems.

Course Outcomes: At the end of this course, students will demonstrate the ability to

1. Obtain discrete representation of LTI systems.
2. Find the state space analysis of discrete time systems.
3. Test and analyze the controllability and observability for discrete time systems
4. Analyze stability of discrete time systems using various methods
5. Design and analyze digital controllers.
6. Design state feedback controllers and observers.

UNIT- I: REPRESENTATION OF DISCRETE TIME SYSTEMS

Basics of Digital Control Systems. Discrete representation of continuous systems. Sample and hold circuit. Mathematical Modeling of sample and hold circuit. Effects of Sampling and Quantization. Choice of sampling frequency. ZOH equivalent.

Z-Transforms, Mapping from s-plane to z plane, Properties of Z-Transforms and Inverse Z Transforms. Pulse Transfer function: Pulse transfer function of closed loop systems. Solution of Discrete time systems. Time response of discrete time system, Steady State errors.

UNIT- II: DISCRETE TIME STATE SPACE ANALYSIS

State space representation of discrete time systems, Conversion of pulse transfer function to state space models and vice-versa, Solving discrete time state space equations, State Transition Matrix, Pulse Transfer Function Matrix. Discretization of continuous time state space equations. Concept of Controllability, stabilizability, observability, reachability – Controllability and observability tests. Effect of pole zero cancellation on the controllability & observability.

UNIT- III: STABILITY ANALYSIS OF DISCRETE TIME SYSTEM

Concept of stability in z-domain, Stability analysis discrete time system: by Jury test, using bilinear transformation.Stability Analysis of discrete time systems using Lyapunov methods.

UNIT- IV: DESIGN OF DIGITAL CONTROL SYSTEM BY CONVENTIONAL METHODS

Design and realization of digital PID Controller, Design of discrete time controllers with bilinear transformation,Design of digital control system with dead beat response, Practical issues with dead beat response design.

UNIT-V: DESIGN STATE FEEDBACK CONTROLLERS AND OBSERVERS

Design of discrete state feedback controllers through pole placement, Design of Discrete Observer for LTI System:Design of full order and reduced observers, Design of observer-based controllers.

TEXT BOOKS:

1. K. Ogata, "Digital Control Engineering", Prentice Hall, Englewood Cliffs, 1995.
2. M. Gopal, "Digital Control Engineering", Wiley Eastern, 1988.
3. V, I, George and C. P. Kurian, Digital Control Systems, CENGAGE Learning, 2012

REFERENCE BOOKS:

1. G. F. Franklin, J. D. Powell and M. L. Workman, "Digital Control of Dynamic Systems", Addison-Wesley,1998.
2. B.C. Kuo, "Digital Control System", Holt, Rinehart and Winston, 1980.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER

EMBEDDED SYSTEMS

IOT ARCHITECTURES AND SYSTEM DESIGN (PE– III)

Course Objectives

1. To Know the definition and basic concepts of IoT
2. Learn the interfacing the IoT and M2M
3. To understand the Architecture of IoT

Course Outcomes: Students will be able to:

1. Integrate the sensors and actuator depending on the applications
2. Interface the IoT and M2M with value chains
3. Write Python programming for Arduino, Raspberry Pi devices
4. Design IoT based systems such as Agricultural IoT, Vehicular IoT etc.,

UNIT - I

IoT introduction: Introduction and definition of IoT, Evolution of IoT, IoT growth, Application areas of IoT, Characteristics of IoT, IoT stack, Enabling technologies, IoT levels, IoT sensing and actuation, Sensing types, Actuator types.

UNIT - II

IoT and M2M: M2M to IoT – A Basic Perspective– Introduction, Differences and similarities between M2M and IoT, SDN and NFV for IoT.M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies.

UNIT - III

IoT Hands-on: Introduction to Arduino Programming, Integration of Sensors and Actuators with Arduino. Introduction to Python programming, Introduction to Raspberry Pi, Interfacing Raspberry Pi with basic peripherals, Implementation of IoT with Raspberry Pi.

UNIT - IV

IoT Architecture: IoT Architecture components, Comparing IoT architectures, A simplified IoT architecture, The core IoT functional stack, IoT data management and compute stack

UNIT - V

IoT System design: Challenges associated with IoT, Emerging pillors of IoT, Agricultural IoT, Vehicular IoT, Healthcare IoT, Smart cities, Transportation and logistics.

TEXT BOOKS:

1. Sudip Misra, Anandarup Mukherjee, Arijit Roy "Introduction to IOT", Cambridge University Press.
2. David Hanes, Gonzalo salgueiro, Patrick Grossetete, Rob barton, Jerome henry "IoT Fundamentals Networking technologies, protocols, and use cases for IoT", Cisco Press

REFERENCE BOOKS:

1. Cuno pfister, "Getting started with the internet of things", O Reilly Media, 2011
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1 st Edition, Apress Publications.
3. "Internet of Things concepts and applications", Wiley
4. Arshdeep Bahga,Vijay Madisetti "Internet of Things A Hands on approach", Universities Press

5. Shriram K Vasudevan, RMD Sundaram, Abhishek S Nagarajan, "Internet of things" John Wiley and Sons.
6. Massimo Banzi, Michael Shiloh Make: Getting Started with the Arduino, Shroff Publisher/Maker Media Publishers.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
DESIGN FOR TESTABILITY (PE – III)

Pre-Requisite: Digital System Design

Course Objectives:

1. To acquire the knowledge of fundamental concepts of testing
2. To provide broad understanding the fault simulation.
3. To illustrate the framework of Built-in-self test and Boundary scan methods.

Course Outcomes: Students will be able to

1. Acquire verification knowledge and test evaluation
2. Design for testability rules and techniques.
3. Utilize the scan architectures for different digital circuits.
4. Acquire the knowledge of design of built-in-self test.

UNIT - I

Introduction to Testing: Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT - II

Logic and Fault Simulation: Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT - III

Testability Measures: SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT - IV

Built-In Self-Test: The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT - V

Boundary Scan Standard: Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK:

1. M.L. Bushnell, V. D. Agrawal, "Essential of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publishers.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breuer and A.D Friedman, Digital Systems and Testable Design", Jaico Publishing House.
2. P. K. Lala, "Digital Circuits Testing and Testability", Academic Press.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
SOC DESIGN (PE – III)

Course Objectives:

1. To learn ASIC design concepts and strategies
2. To know the NISC applications and advantages
3. To familiar with simulation and synthesis process

Course Outcomes: At the end of the course, students will be able to:

1. Identify and formulate a given problem in the framework of SoC based design approaches
2. Design SoC based system for engineering applications
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

UNIT - I

ASIC: Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP)concepts.

UNIT - II

NISC: NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction- set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT - III

Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT - IV

Low power SoC design / Digital system Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

UNIT - V

Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report, analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

TEXT BOOKS:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006

REFERENCE BOOKS

1. Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000
2. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
3. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
HARDWARE AND SOFTWARE CO-DESIGN (PE – IV)

Course Objectives:

1. To Know the Co-design Issues, prototype and emulation techniques
2. To learn Architecture specific techniques
3. To know the different tool for design

Course Outcomes: Students will be able to:

1. Acquire the knowledge on various models of Co-design.
2. Explore the interrelationship between Hardware and software in a embedded system
3. Acquire the knowledge of firmware development process and tools during Co-design.
4. Implement validation methods and adaptability.

UNIT - I

Co-Design Issues: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.
Co-Synthesis Algorithms: Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II

Prototyping and Emulation: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Target Architectures: Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V

Languages for System – Level Specification and Design-I: System – level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II: Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.

REFERENCE BOOKS

1. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, Kluwer Academic Publishers, 2002.
2. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
SECURE NETWORKS (PE -IV)

Course Objectives:

1. To underlying principles and techniques for network and communication security.
2. To learn practical examples of security problems and principles for countermeasures
3. To provide cryptographic methods, protocols and applications.

Course Outcomes: At the end of the course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

UNIT -I:

Security: Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

UNIT -II

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

UNIT -III

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

UNIT -IV

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

UNIT -V

Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition

REFERENCE BOOKS:

1. Christopher M. King, Ertem Osmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Press,
2. Stephen Northcutt, Leny Zeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS PHYSICAL DESIGN AUTOMATION (PE -IV)

Course Objectives:

1. To understand the concepts of Physical Design Process (partitioning, Floor planning etc.,)
2. To know the concepts of design optimization algorithms and their application
3. To understand the clock and power design concepts

Course Outcomes: At the end of the course, students will be able to:

1. Implement automation process for VLSI System design.
2. Familiarize to use various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

UNIT - I

Introduction to VLSI Physical Design Automation: Design Representation, VLSI Design Styles, and VLSI Physical Design automation.

UNIT - II

Partitioning, Floor planning, Pin Assignment, Standard cell, Performance issues in circuit layout, delay models, Layout styles.

UNIT - III

Placement: Problem formulation, classification, Simulation based placement algorithms, Partitioning based placement algorithms, Time driven and performance driven placement.

UNIT - IV

Global routing: Problem formulation, classification of global routing, Maze routing algorithms, Line-Probe algorithms, and shortest path based algorithms, Steiner Tree based algorithms, Integer programming based approach, Performance driven routing.

Detailed Routing: Problem formulation, classification, Single layer, two layer, three layer and Multi-Layer channel routing, Algorithms, Switch box routing.

UNIT - V

Over the Cell Routing - Single layer and two-layer routing: Over the cell routing, Two Layer, Three Layer and Multi-Layer OTC Routing.

Via Minimization: Constraint and Unconstrained via minimization.

Clock and Power Routing: Clocking schemes, design considerations for the clock, Problem formulation, Clock routing algorithms, Skew and Delay reduction by Pin Assignment, Multiple clock routing, Power and Ground Routing

TEXT BOOKS:

1. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005,
2. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley& Sons (Asia) Pvt. Ltd.

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design: Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia

ELLENKI COLLEGE OF ENGINEERING AND TECHNOLOGY

M.TECH.- I YEAR- II SEMESTER
EMBEDDED SYSTEMS
ARM MICROCONTROLLERS LAB (Lab – III)

Course Outcomes: At the end of the laboratory work, students will be able to:

1. Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
2. Develop prototype codes using commonly available on and off chip peripherals on the Cortex M3 and DSP development boards.

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the SysTicktimer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.